UNIT–1: Functional Blocks & ISA (Q1–Q17)

1. The main function of the CPU is to
   A) Store data
   B) Control I/O devices
   C) Execute instructions
   D) Manage memory
   ✅ **Answer: C**
2. Which unit performs arithmetic and logical operations?
   A) CU
   B) ALU
   C) Register
   D) Memory
   ✅ **Answer: B**
3. The Program Counter (PC) holds
   A) Current instruction
   B) Next instruction address
   C) Operand address
   D) Result
   ✅ **Answer: B**
4. Which register stores the instruction currently being executed?
   A) PC
   B) MAR
   C) IR
   D) MDR
   ✅ **Answer: C**
5. RTL stands for
   A) Register Transfer Language
   B) Real Time Logic
   C) Reduced Transfer Logic
   D) Runtime Language
   ✅ **Answer: A**
6. Which step comes first in instruction execution cycle?
   A) Decode
   B) Execute
   C) Fetch
   D) Write back
   ✅ **Answer: C**
7. Addressing mode where operand is part of instruction is
   A) Direct

B) Immediate
C) Indirect
D) Indexed
✅ **Answer: B**

8. Which addressing mode uses a register to hold operand?
A) Immediate
B) Direct
C) Register
D) Indexed
✅ **Answer: C**

9. ISA defines
A) Circuit design
B) Programming language
C) Hardware–software interface
D) Memory size
✅ **Answer: C**

10. Which is a CISC processor?
A) ARM
B) MIPS
C) RISC-V
D) x86
✅ **Answer: D**

11. Which CPU type has fixed-length instructions?
A) x86
B) ARM
C) CISC
D) 8086
✅ **Answer: B**

12. Control unit mainly
A) Stores data
B) Executes arithmetic
C) Generates control signals
D) Performs I/O
✅ **Answer: C**

13. Which register interfaces CPU and memory?
A) PC
B) IR
C) MAR
D) SP
✅ **Answer: C**

14. Instruction set consists of
A) Only arithmetic instructions
B) Hardware circuits
C) Machine-level commands

D) OS services

✅ **Answer: C**

15. Which memory is fastest?
    A) Cache
    B) RAM
    C) Register
    D) ROM
    ✅ **Answer: C**
16. Which unit synchronizes CPU operations?
    A) Clock
    B) ALU
    C) Register
    D) Memory
    ✅ **Answer: A**
17. Indexed addressing is useful for
    A) Constants
    B) Arrays
    C) Stack
    D) I/O
    ✅ **Answer: B**

UNIT–2: Data Representation & Arithmetic (Q18–Q40)

18. Most commonly used signed number system is
    A) Sign magnitude
    B) 1's complement
    C) 2's complement
    D) Excess-3
    ✅ **Answer: C**
19. Range of n-bit 2's complement number is
    A) -2^n to 2^n
    B) $-(2^{n-1})$ to $(2^{n-1} - 1)$
    C) $-(2^n)$ to $(2^n - 1)$
    D) 0 to 2^n
    ✅ **Answer: B**
20. Floating point standard used is
    A) ASCII
    B) Unicode
    C) IEEE-754
    D) EBCDIC
    ✅ **Answer: C**

21. Fixed-point representation is mainly used for
    A) Real numbers
    B) Integers
    C) Characters
    D) Strings
    ✅ **Answer: B**
22. ASCII is a
    A) 16-bit code
    B) 8-bit code
    C) 7-bit code
    D) 32-bit code
    ✅ **Answer: C**
23. Unicode supports
    A) Only English
    B) Only numbers
    C) Multiple languages
    D) Only symbols
    ✅ **Answer: C**
24. Subtraction in binary is done using
    A) 1’s complement
    B) 2’s complement
    C) Sign bit
    D) XOR
    ✅ **Answer: B**
25. Ripple carry adder disadvantage is
    A) Complex design
    B) High cost
    C) Slow speed
    D) Large size
    ✅ **Answer: C**
26. Carry look-ahead adder improves
    A) Cost
    B) Accuracy
    C) Speed
    D) Power
    ✅ **Answer: C**
27. Booth’s algorithm is used for
    A) Division
    B) Floating point addition
    C) Signed multiplication
    D) Addition
    ✅ **Answer: C**
28. Shift-and-add method is used for
    A) Division
    B) Multiplication

C) Subtraction
D) Comparison
✅ **Answer: B**

29. Carry save multiplier improves
A) Memory usage
B) Partial product addition
C) Control signals
D) Division speed
✅ **Answer: B**

30. Restoring division restores
A) Quotient
B) Remainder
C) Partial remainder
D) Dividend
✅ **Answer: C**

31. Non-restoring division is
A) Slower
B) Faster
C) Same as restoring
D) Not used
✅ **Answer: B**

32. Floating point number consists of
A) Sign, mantissa, exponent
B) Integer and fraction
C) Only exponent
D) Only mantissa
✅ **Answer: A**

33. Overflow occurs when
A) Result fits in bits
B) Carry is lost
C) Sign changes incorrectly
D) Both B and C
✅ **Answer: D**

34. Ripple carry adder delay increases with
A) Voltage
B) Bit width
C) Clock speed
D) Power
✅ **Answer: B**

35. IEEE-754 single precision uses
A) 32 bits
B) 64 bits
C) 16 bits
D) 128 bits
✅ **Answer: A**

36. Exponent bias in single precision is
    A) 64
    B) 127
    C) 255
    D) 1023
    ✅ **Answer: B**
37. Character ‘A’ in ASCII is
    A) 41H
    B) 42H
    C) 61H
    D) 21H
    ✅ **Answer: A**
38. Carry look-ahead uses
    A) Sequential carry
    B) Generate and propagate
    C) Shift register
    D) Decoder
    ✅ **Answer: B**
39. Sign bit for negative number is
    A) 0
    B) 1
    C) Depends
    D) Undefined
    ✅ **Answer: B**
40. Mantissa is also called
    A) Fraction
    B) Exponent
    C) Integer
    D) Base
    ✅ **Answer: A**

UNIT–3: x86 & CPU Design (Q41–Q55)

41. x86 architecture belongs to
    A) RISC
    B) CISC
    C) EPIC
    D) SIMD
    ✅ **Answer: B**
42. x86 instructions are
    A) Fixed length
    B) Variable length

C) Always 32-bit
D) Always 64-bit
✅ **Answer: B**

43. Hardwired control unit is
A) Slow and flexible
B) Fast and inflexible
C) Slow and complex
D) Micro-coded
✅ **Answer: B**

44. Micro-programmed control uses
A) Logic gates
B) Control memory
C) Cache
D) Registers
✅ **Answer: B**

45. Micro-instructions are stored in
A) RAM
B) ROM
C) Cache
D) Control memory
✅ **Answer: D**

46. Hypothetical CPU is used to
A) Replace real CPUs
B) Teach concepts
C) Increase speed
D) Design OS
✅ **Answer: B**

47. DRAM stores data as
A) Flip-flops
B) Capacitors
C) Registers
D) Transistors only
✅ **Answer: B**

48. SRAM is faster than DRAM because it
A) Needs refresh
B) Uses capacitors
C) Uses flip-flops
D) Is cheaper
✅ **Answer: C**

49. ROM is
A) Volatile
B) Non-volatile
C) Cache
D) Register
✅ **Answer: B**

50. Memory organization involves
    A) Address decoding
    B) Instruction execution
    C) ALU design
    D) I/O control
    ✅ **Answer: A**
51. Byte-addressable memory means
    A) Each address stores a word
    B) Each address stores a byte
    C) Each byte stores address
    D) Only integers stored
    ✅ **Answer: B**
52. Control signals are generated by
    A) ALU
    B) Memory
    C) Control Unit
    D) Register
    ✅ **Answer: C**
53. Microprogramming increases
    A) Speed
    B) Hardware cost
    C) Flexibility
    D) Power
    ✅ **Answer: C**
54. x86 supports
    A) Few addressing modes
    B) Many addressing modes
    C) Only register mode
    D) Only immediate mode
    ✅ **Answer: B**
55. DRAM requires
    A) No refresh
    B) Periodic refresh
    C) Battery backup
    D) Cache
    ✅ **Answer: B**

UNIT–4: I/O & Interrupts (Q56–Q70)

56. I/O devices are slower than
    A) Memory
    B) CPU

C) Cache
D) Register
✅ **Answer: B**

57. Program-controlled I/O uses
A) DMA
B) Polling
C) Interrupts
D) Cache
✅ **Answer: B**

58. Interrupt-driven I/O improves
A) CPU utilization
B) Hardware cost
C) Memory size
D) Speed of ALU
✅ **Answer: A**

59. DMA allows data transfer between
A) CPU and memory
B) I/O and CPU
C) I/O and memory
D) Cache and CPU
✅ **Answer: C**

60. DMA controller temporarily becomes
A) Slave
B) CPU
C) Bus master
D) Cache
✅ **Answer: C**

61. Privileged instructions are executed in
A) User mode
B) Kernel mode
C) Cache mode
D) DMA mode
✅ **Answer: B**

62. Non-privileged instructions run in
A) Kernel mode
B) User mode
C) Supervisor mode
D) Interrupt mode
✅ **Answer: B**

63. Software interrupt is also called
A) Trap
B) IRQ
C) DMA
D) Poll
✅ **Answer: A**

64. Exceptions are caused by
    A) External devices
    B) Program errors
    C) DMA
    D) Cache
    ✅ **Answer: B**
65. Interrupt causes
    A) Infinite loop
    B) Context switching
    C) Deadlock
    D) Cache miss
    ✅ **Answer: B**
66. Process states include
    A) Fetch, decode
    B) Ready, running, blocked
    C) Load, store
    D) Read, write
    ✅ **Answer: B**
67. USB stands for
    A) Universal Serial Bus
    B) Unified System Bus
    C) Universal System Base
    D) User Serial Bus
    ✅ **Answer: A**
68. SCSI is mainly used for
    A) Keyboard
    B) Storage devices
    C) Monitor
    D) Mouse
    ✅ **Answer: B**
69. I/O interface contains
    A) ALU
    B) Registers
    C) Cache
    D) Decoder
    ✅ **Answer: B**
70. Status register indicates
    A) Data
    B) Device condition
    C) Address
    D) Instruction
    ✅ **Answer: B**

UNIT–5: Pipelining & Parallel Processors (Q71–Q85)

71. Pipelining improves
    A) Latency
    B) Throughput
    C) Memory size
    D) Instruction size
    ✅ **Answer: B**
72. Ideal pipeline speedup equals
    A) Clock speed
    B) Number of stages
    C) Memory size
    D) CPI
    ✅ **Answer: B**
73. Structural hazard occurs due to
    A) Branches
    B) Resource conflict
    C) Data dependency
    D) Cache miss
    ✅ **Answer: B**
74. Data hazard occurs when
    A) Same resource used
    B) Instruction depends on previous result
    C) Branch instruction
    D) Interrupt
    ✅ **Answer: B**
75. Control hazard is caused by
    A) Arithmetic
    B) Memory access
    C) Branch instruction
    D) DMA
    ✅ **Answer: C**
76. Pipeline stage example is
    A) Store
    B) Fetch
    C) Compare
    D) Jump
    ✅ **Answer: B**
77. Parallel processors execute
    A) One instruction at a time
    B) Multiple instructions simultaneously
    C) Only I/O
    D) Only memory access
    ✅ **Answer: B**

78. SMP stands for
    A) Simple Memory Processor
    B) Shared Memory Processor
    C) Symmetric Multiprocessor
    D) Serial Multi Processor
    ✅ **Answer: C**
79. Cache coherency ensures
    A) Faster cache
    B) Same data view
    C) Larger cache
    D) Less memory
    ✅ **Answer: B**
80. MESI protocol stands for
    A) Modified, Exclusive, Shared, Invalid
    B) Memory, Exclusive, Shared, Invalid
    C) Modified, Efficient, Simple, Invalid
    D) Main, Extra, Shared, Internal
    ✅ **Answer: A**
81. Throughput is measured as
    A) Time per instruction
    B) Instructions per second
    C) Clock period
    D) CPI
    ✅ **Answer: B**
82. CPI stands for
    A) Cycles Per Instruction
    B) Cost Per Instruction
    C) Clock Per Interrupt
    D) Cache Per Instruction
    ✅ **Answer: A**
83. Pipeline flushing occurs due to
    A) Arithmetic
    B) Branch misprediction
    C) Cache hit
    D) DMA
    ✅ **Answer: B**
84. Parallel memory access causes
    A) Deadlock
    B) Conflict
    C) Coherency issue
    D) Overflow
    ✅ **Answer: C**
85. Speedup is limited by
    A) Moore’s law
    B) Amdahl’s law

C) Ohm’s law
D) Newton’s law
✅ **Answer: B**

UNIT–6: Memory Organization & Cache (Q86–Q100)

86. Memory interleaving improves
A) Capacity
B) Access speed
C) Cost
D) Power
✅ **Answer: B**
87. Memory hierarchy is based on
A) Cost only
B) Speed and size
C) Voltage
D) Software
✅ **Answer: B**
88. Cache memory exploits
A) Temporal locality
B) Spatial locality
C) Both
D) None
✅ **Answer: C**
89. Cache is placed between
A) CPU and I/O
B) CPU and RAM
C) RAM and disk
D) Disk and I/O
✅ **Answer: B**
90. Direct mapping maps a block to
A) Any line
B) One specific line
C) Multiple lines
D) Set
✅ **Answer: B**
91. Fully associative mapping allows
A) One location
B) Fixed mapping
C) Any cache line
D) No mapping
✅ **Answer: C**

92. Set-associative mapping is a combination of
    A) Cache and RAM
    B) Direct and associative
    C) FIFO and LRU
    D) Write through and write back
    ✅ **Answer: B**
93. LRU replacement replaces
    A) First block
    B) Random block
    C) Least recently used block
    D) Largest block
    ✅ **Answer: C**
94. FIFO replaces
    A) Latest block
    B) Oldest block
    C) Random block
    D) Largest block
    ✅ **Answer: B**
95. Write-through policy updates
    A) Cache only
    B) Memory only
    C) Cache and memory
    D) Disk
    ✅ **Answer: C**
96. Write-back updates memory
    A) Immediately
    B) On replacement
    C) Never
    D) Periodically
    ✅ **Answer: B**
97. Cache miss penalty is
    A) Cache access time
    B) Time to fetch from memory
    C) CPU speed
    D) Hit rate
    ✅ **Answer: B**
98. Larger block size increases
    A) Miss rate always
    B) Spatial locality
    C) Latency
    D) Power
    ✅ **Answer: B**
99. Tag field is used to
    A) Store data
    B) Identify memory block

C) Store index
D) Store offset
✅ **Answer: B**

100. Valid bit indicates
A) Cache size
B) Correct data presence
C) Dirty data
D) Replacement order
✅ **Answer: B**

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