Digital IC Logic Families

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Introduction

- Basically, there are two types of semiconductor devices: bipolar and unipolar.
- Based on these devices, digital integrated circuits have been made which are commercially available.
- Various digital functions are being fabricated in a variety of forms using bipolar and unipolar technologies.
- A group of compatible ICs with the same logic levels and supply voltages for performing various logic functions have been fabricated using a specific circuit configuration which is referred to as a *logic family.*
- *Logic Families are classified into two types:*
  - *Bipolar logic family*
  - *Unipolar Logic Family*

Bipolar Logic Families

- The main elements of a bipolar IC are resistors, diodes (which are also capacitors) and transistors. Basically, there are two types of operations in bipolar ICs:

1. Saturated, and

2. Non-saturated.

- In saturated logic, the transistors in the IC are driven to saturation, whereas in the case of non-saturated logic, the transistors are not driven into saturation.
- The saturated bipolar logic families are:
    1. Resistor–transistor logic (RTL),
    2. Direct–coupled transistor logic (DCTL),
    3. Integrated–injection logic (I^2L)
    4. Diode–transistor logic (DTL),
    5. High–threshold logic (HTL), and
    6. Transistor-transistor logic (TTL).
- The non-saturated bipolar logic families are:
    1. Schottky TTL, and
    2. [illegible]ed logic (ECL).

Unipolar Logic Families

- MOS devices are unipolar devices and only MOSFETs are employed in MOS logic circuits.
- The MOS logic families are:
- 1. PMOS,
- 2. NMOS, and
- 3. CMOS
- While in PMOS only *p-channel MOSFETs are used and in NMOS only n-channel MOSFETs* are used, in complementary MOS (CMOS), both *p- and n-channel MOSFETs are employed* and are fabricated on the same silicon chip.

CHARACTERISTICS OF DIGITAL ICs

- With the widespread use of ICs in digital systems and with the development of various technologies for the fabrication of ICs, it has become necessary to be familiar with the characteristics of IC logic families and their relative advantages and disadvantages.
- The various characteristics of digital ICs used to compare their performances are:
  1. Speed of operation,
  2. Power dissipation,
  3. Figure of merit,
  4. Fan-in
  5. Fan-out,
  6. Current and voltage parameters,
  7. Noise immunity,
  8. Operating temperature range,
  9. Power supply requirements

Speed of Operation

- The speed of a digital circuit is specified in terms of the propagation delay time. The input and output waveforms of a logic gate are shown in Fig. 4.1. The delay times are measured between the 50 per cent voltage levels of input and output waveforms. There are two delay times: *tpLH*, *tpHL.*
- when the output goes from the HIGH state to the LOW state and corresponding to the output making a transition from the LOW state to the HIGH state. The propagation delay time of the logic gate is taken as the average of these two delay times.
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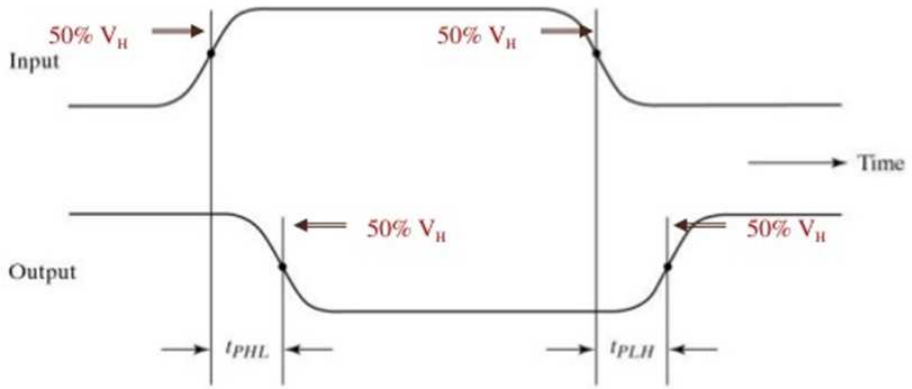


Power Dissipation

- This is the amount of power dissipated in an IC. It is determined by the current, I_{CC} that it draws from the V_{CC} supply, and is given by *VCC x ICC. ICC* is the average value of *Icc*(0) and *ICC*(1). This power is specified in mill watts.

Figure of Merit

- The figure of merit of a digital IC is defined as the product of speed and power. The speed is specified in terms of propagation delay time expressed in nanoseconds.

  Figure of merit = propagation delay time (*ns) x power (mW)*

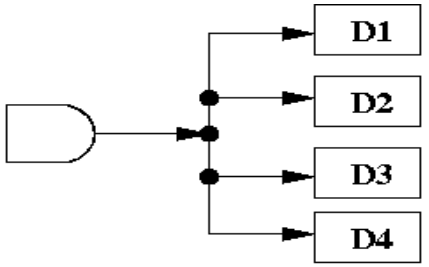
- It is specified in pico joules (*ns x mW = pJ)*
- A low value of speed-power product is desirable. In a digital circuit, if it is desired to have high speed, i.e. low propagation delay, then there is a corresponding increase in the power dissipation and vice-versa.

Fan-in:

- Fan-in is the number of inputs to a gate. For a two inputs gate, fan-in is two; and for a four inputs gate, fan-in is 4.

Fan-out:

- This is the number of similar gates which can be driven by a gate. High fan-out is advantageous because it reduces the need for additional drivers to drive more gates.



Current and Voltage Parameters

V_{IH}(min)—High-Level Input Voltage. The minimum voltage level required for a logical 1 at an *input*. Any voltage below this level will not be accepted as a HIGH by the logic circuit.

V_{IL}(max)—Low-Level Input Voltage. The maximum voltage level required for a logic 0 at an *input*. Any voltage above this level will not be accepted as a LOW by the logic circuit.

V_{OH}(min)—High-Level Output Voltage. The minimum voltage level at a logic circuit *output* in the logical 1 state under defined load conditions.

V_{OL}(max)—Low-Level Output Voltage. The maximum voltage level at a logic circuit *output* in the logical 0 state under defined load conditions.

I_{IH}—High-Level Input Current. The current that flows into an input when a specified high-level voltage is applied to that input.

I_{IL}—Low-Level Input Current. The current that flows into an input when a specified low-level voltage is applied to that input.

I_{OH}—High-Level Output Current. The current that flows from an output in the logical 1 state under specified load conditions.

I_{OL}—Low-Level Output Current. The current that flows from an output in the logical 0 state under specified load conditions.

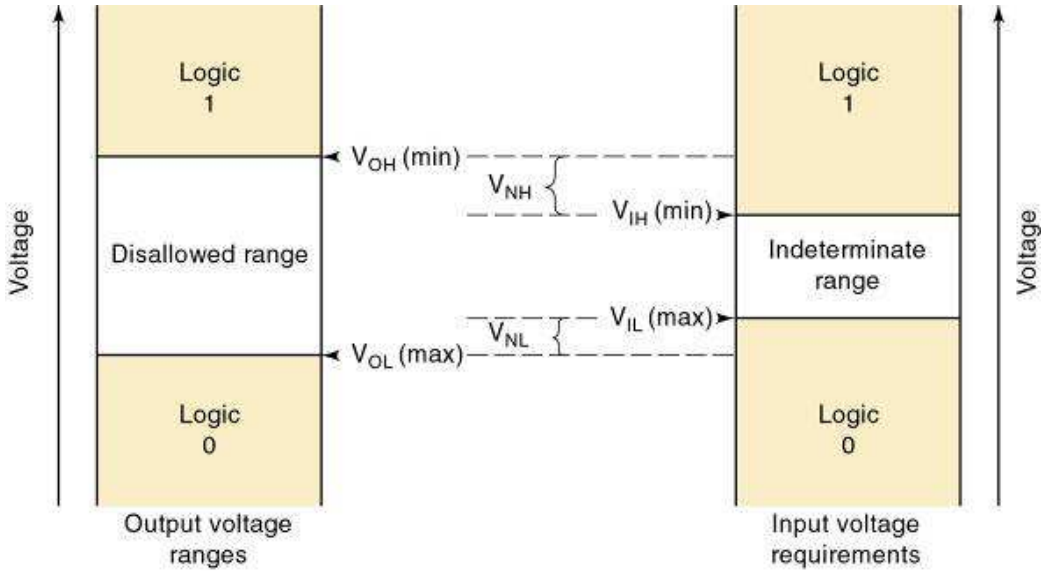
- **Noise immunity** refers to the circuit's ability to tolerate noise without changes in output voltage.
  - A quantitative measure is called **noise margin**.

High-state noise margin:

$$V_{NH} = V_{OH}(\text{min}) - V_{IH}(\text{min})$$
$$= 2.4\,\text{V} - 2.0\,\text{V} = 0.4\,\text{V}$$

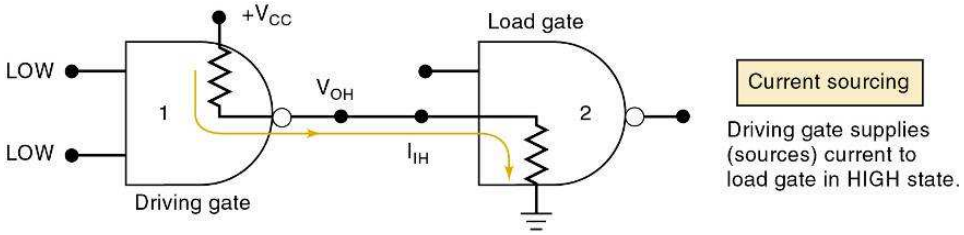
Low-state noise margin:

$$V_{NL} = V_{IL}(\text{max}) - V_{OL}(\text{max})$$



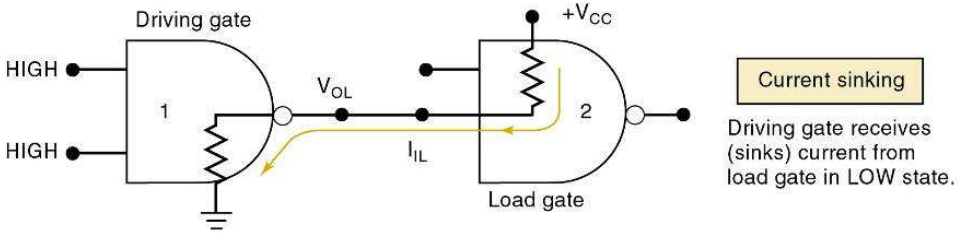
- **Operating Temperature**
- The temperature range in which an IC functions properly must be known. The accepted temperature ranges are: 0 to + 70 °C for consumer and industrial applications and –55 °C to + 125 °C for military purposes.
- **Power Supply Requirements**
- The supply voltage(s) and the amount of power required by an IC are important characteristics required to choose the proper power supply.

Current Sourcing



- **Current-sourcing** action.
  - When the output of gate 1 is HIGH, it supplies current I_{IH} to the input of gate 2.
    - Which acts essentially as a resistance to ground.
  - The output of gate 1 is acting as a *source* of current for the gate 2 input.

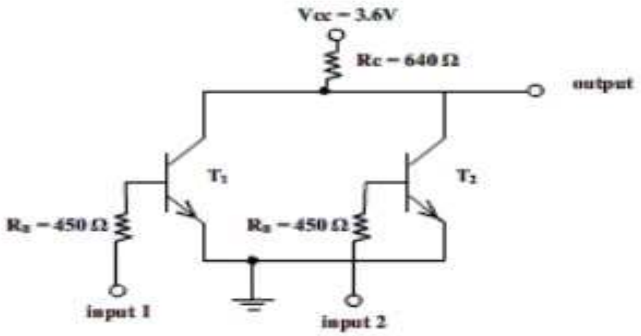
Current Sinking



Current-sinking action.

- Input circuitry of gate 2 is represented as a resistance tied to $+V_{CC}$ —the positive terminal of a power supply.
- When gate 1 output goes LOW, current will flow from the input circuit of gate 2 back through the output resistance of gate 1, to ground.
- Circuit output that drives the input of gate 2 must be able to *sink* a current, I_{IL} , coming from that input.

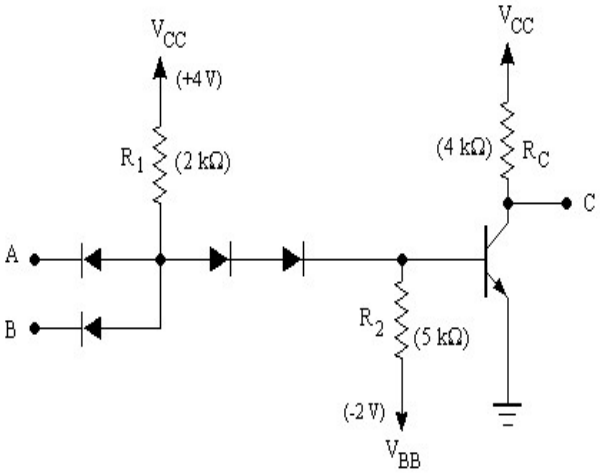
Register-Transistor Logic(RTL)



V1	V2	T1	T2	Output
Logic 0	Logic 0	Cut-off	Cut-off	Logic 1
Logic 0	Logic 1	Cut-off	saturation	Logic 0
Logic 1	Logic 0	saturation	Cut-off	Logic 0
Logic 1	Logic 1	saturation	saturation	Logic 0

- The resistor-transistor logic, also termed as RTL, was most popular kind of logic before the invention of IC fabrication technologies.
- As its name suggests, RTL circuits mainly consists of resistors and transistors that comprises RTL devices. The basic RTL device is a NOR gate, shown in figure aside.
- *Inputs to the NOR gate shown above are 'input1' & 'input2'. The inputs applied at these terminals represent either logic level HIGH (1) or LOW (0).*
- *The logic level LOW is the voltage that drives corresponding transistor in cut-off region, while logic level HIGH drives it into saturation region.*
- *If both the inputs are LOW, then both the transistors are in cut-off i.e. they are turned-off. Thus, voltage Vcc appears at output I.e. HIGH.*
- *If either transistor or both of them are applied HIGH input, the voltage Vcc drops across Rc and output is LOW. RTL family is characterized by poor noise margin, poor fan-out capability, low speed and high power dissipation. Due to these undesirable characteristics, this family is now obsolete.*

Diode Transistor Logic



The diode-transistor logic, also termed as DTL, replaced RTL family because of greater fan-out capability and more noise margin.

As its name suggests, DTL circuits mainly consists of diodes and transistors that comprises DTL devices.

The basic DTL device is a NAND gate, shown aside.

Three inputs to the gate are applied through three diodes viz. D1, D2 and D3. The diode will conduct only when corresponding input is LOW.

If any of the diode is conducting i.e. when at least one input is LOW, the voltage at cathode of didoe DA is such that it keeps transistor T in cut-off and subsequently, output of transistor is HIGH.

If all inputs are HIGH, all diodes are non-conducting, transistor T is in saturation, and its output is LOW.

Due to number of diodes used in this circuit, the speed of the circuit is significantly low. Hence this family of logic gates is modified to transistor-transistor logic i.e. TTL family.

DTL (Diode Transistor Logic)

Inputs		Diodes		Transistor Output	
A	B	D1	D2	T	C
Logic 0	Logic 0	Forward biased	Forward biased	Cut-off	Logic 1
Logic 0	Logic 1	Forward biased	Reverse Biased	Cut-off	Logic 1
Logic 1	Logic 0	Reverse Biased	Forward biased	Cut-off	Logic 1
Logic 1	Logic 1	Reverse Biased	Reverse Biased	Saturation	Logic 0

Advantages:

1. Fan-out is high
2. Power dissipation is 8-12mW.
3. Noise immunity is good

Disadvantages:

1. More Elements are required
2. Propagation delay is more and hence the speed of operation is less.

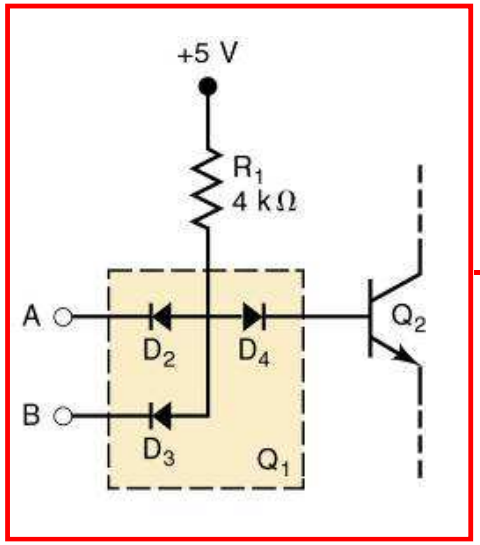
Transistor-Transistor Logic(TTL)

- TTL family is a modification to the DTL. It has come to existence so as to overcome the speed limitations of DTL family.
- Standard TTLs are available in various forms:

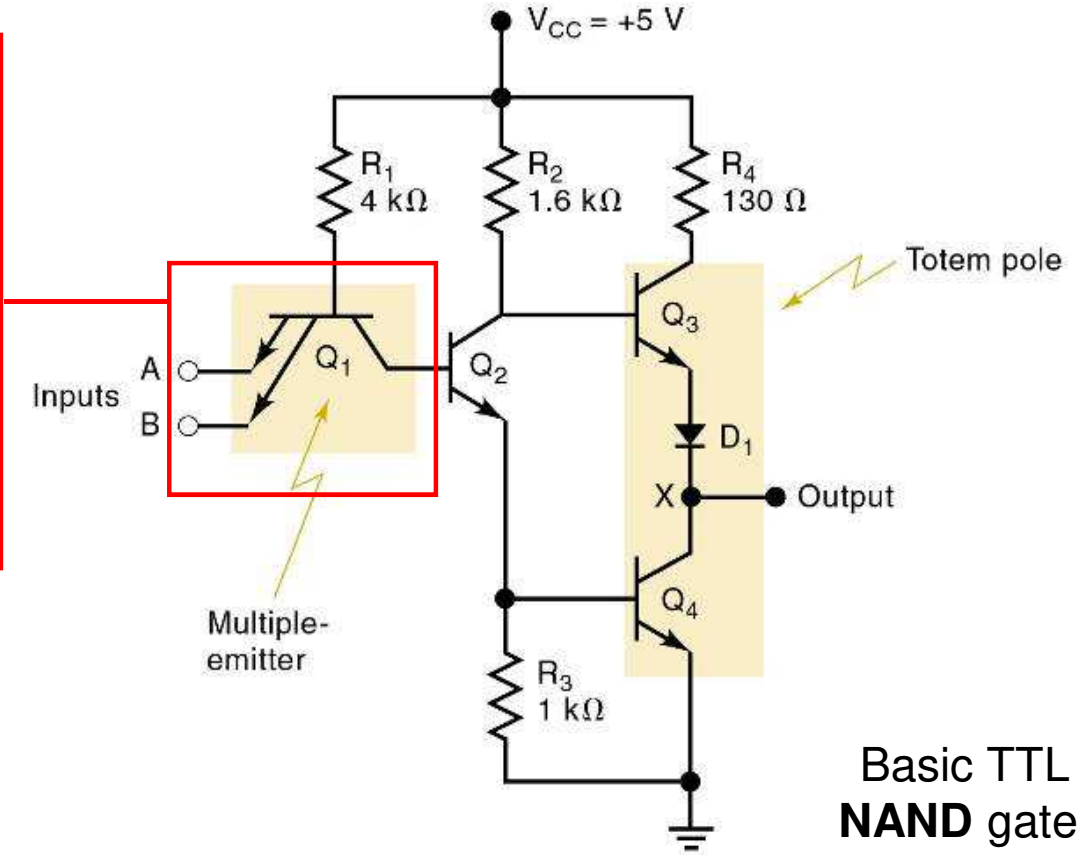
1. TTL with passive pull-up
2. TTL with totem-pole output
3. TTL with open Collector output
4. Tristate TTL.

TTL with Totem-pole Output

The basic TTL logic circuit is the NAND gate.

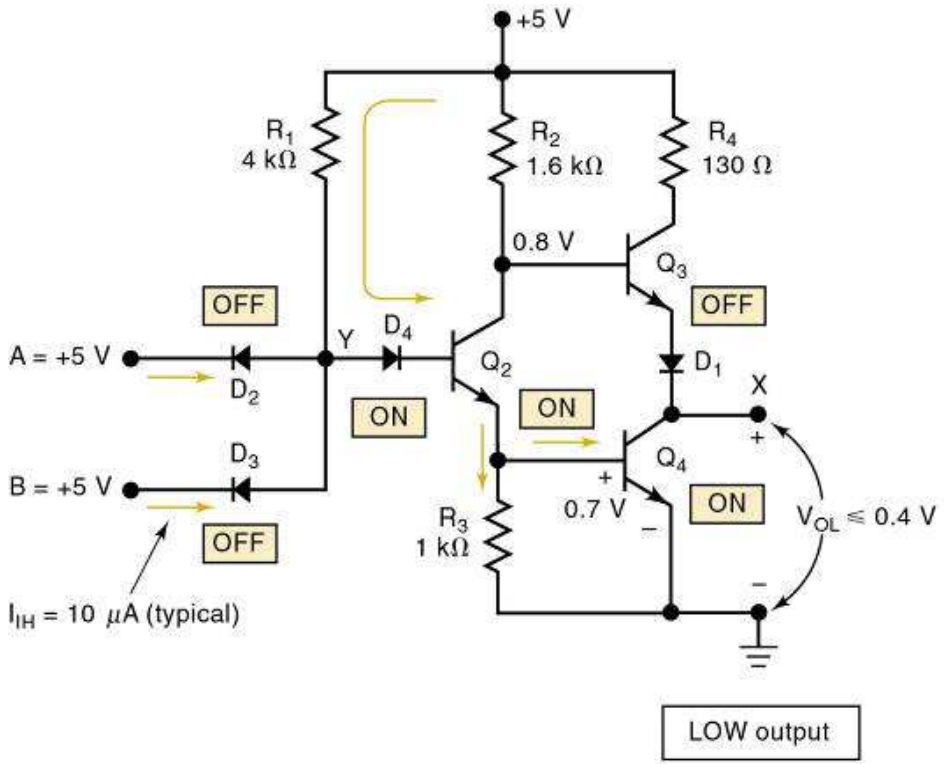


Diode equivalent for Q_1 .



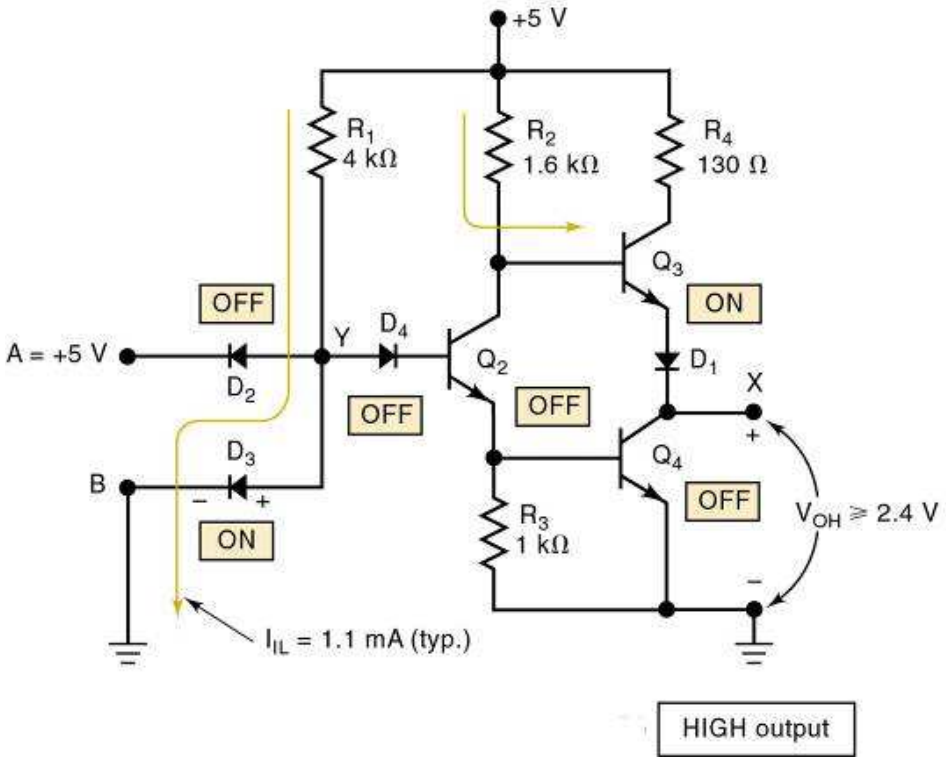
Basic TTL **NAND** gate.

TTL NAND gate LOW output



Input conditions	Output conditions
A and B are both HIGH (≥ 2 V)	Q_3 OFF
Input currents are very low I_{IH} = 10 μA	Q_4 ON so that V_X is LOW (≤ 0.4 V)

TTL NAND gate HIGH output

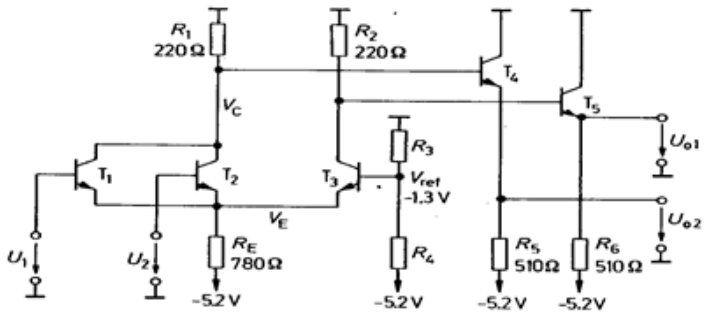


Input conditions	Output conditions
A or B or both are LOW ($\leq$ 0.8 V)	Q_4 OFF
Current flows back to ground through LOW input terminal. I_{IL} = 1.1 mA	Q_3 acts as emitter-follower and $V_{OH} \geq$ 2.4 V, typically 3.6 V

Operation of TTL Nand Gate

Inputs		Transistor T1		Transistors T2 and T4	Transistor T3	Output Y
A	B	Emitter Junction A	Emitter Junction B			
Logic 0	Logic 0	Forward Biased	Forward Biased	Cut-off	Saturation	Logic 1
Logic 0	Logic 1	Forward Biased	Reverse Biased	Cut-off	Saturation	Logic 1
Logic 1	Logic 0	Reverse Biased	Forward Biased	Cut-off	Saturation	Logic 1
Logic 1	Logic 1	Reverse Biased	Reverse Biased	Saturation	Cut-off	Logic 0

Emitter Coupled Logic



- *Figure* shows a typical ECL gate. Transistors T_2 and T_3 form a differential amplifier.
- A constant potential V_{ref} is applied to the base of T_3 via the voltage divider.
- If all the input voltages are in the L state, transistors T_1 and T_2 are turned off.
- The emitter current in this case flows via transistor T_3, producing a voltage drop across R_2 .
- Output voltage U_{01} is therefore in the L state, U_{02} in the H state.
- When at least one input level goes high, the output states are reversed.
- Positive logic gives an or operation for U_{01} and an nor operation for U_{02} .

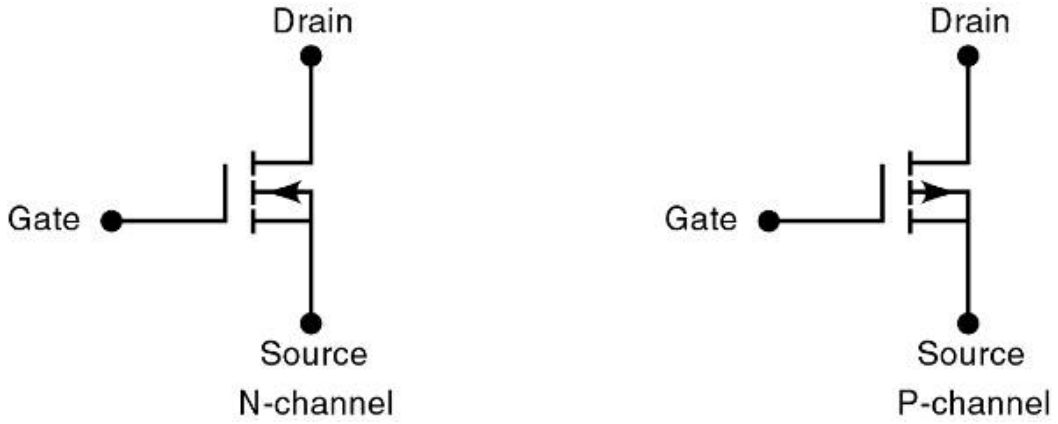
Inputs		Transistors			Transistors		Output	
U2	U1	T2	T1	T3	T4	T5	Uo1(or)	Uo2(Nor)
Logic 0	Logic 0	Cut-off	Cut-off	Active	Active	Cut-off	Logic 0	Logic 1
Logic 0	Logic 1	Cut-off	Active	Cut-off	Cut-off	Active	Logic 1	Logic 0
Logic 1	Logic 0	Active	Cut-off	Cut-off	Cut-off	Active	Logic 1	Logic 0
Logic 1	Logic 1	Active	Active	Cut-off	Cut-off	Active	Logic 1	Logic 0

Characteristics:

1. Less Propagation Delay time.
2. Poor Noise Margin.
3. Power dissipation 40-55 mW.
4. Fan-out is 25.

CMOS Logic

- There are presently two general types of MOSFETs—*depletion* and *enhancement.*
  - MOS ICs use enhancement MOSFETs exclusively.

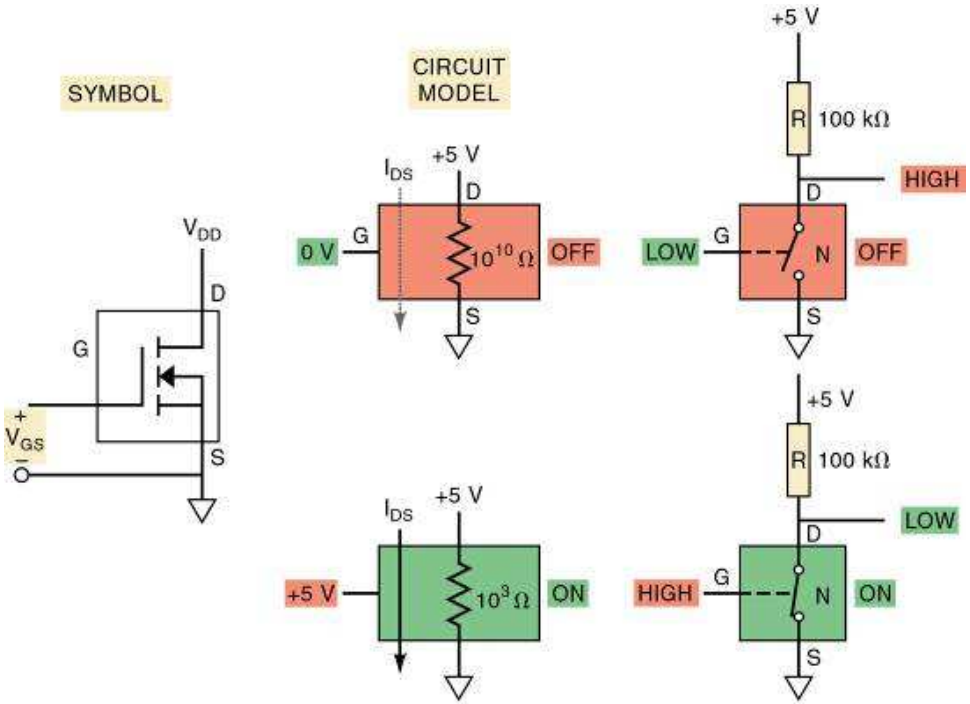


The direction of the arrow indicates either P- or N-channel. The symbols show a broken line between the *source* and the *drain* to indicate there is *normally* no conducting channel between these electrodes.

- An N-channel MOSFET is the basic element in a family of devices known as **N-MOS**.
  - Drain is always biased positive relative to the source.

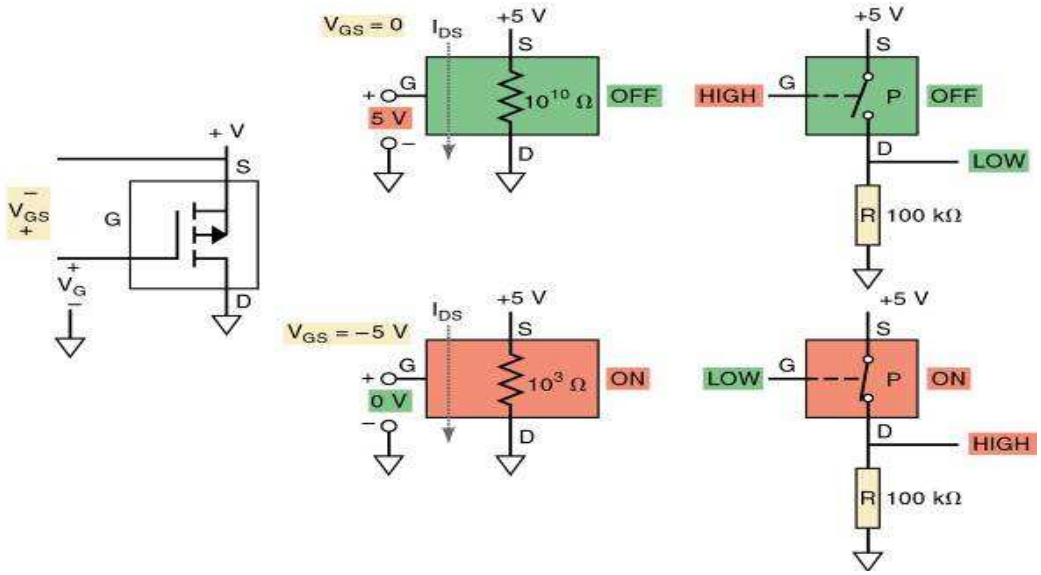
Basic N-MOSFET Switch

- Gate-to-source voltage V_{GS} is the input voltage.
  - Used to control resistance between drain & source.
    - Determines whether the device is on or off.



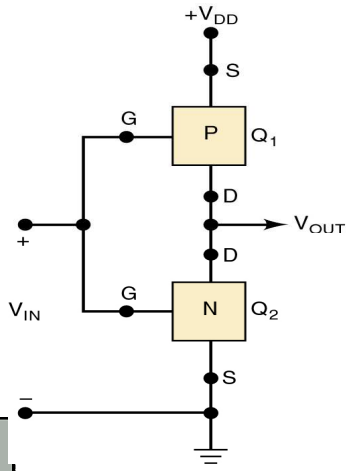
Basic P-MOSFET Switch

- The P-channel MOSFET—**P-MOS**—operates in the same manner as the N-channel.
  - Except that it uses voltages of opposite polarity.
- The drain is connected to the lower side of the circuit so it is biased with a more negative voltage relative to the source.
- To turn the P-MOSFET ON, a voltage *lower* than the source by V_T must be applied to the gate.
  - Voltage at the gate, relative to the source, must be negative.



CMOS Inverter

- P-MOS & N-MOS circuits began to dominate the LSI and VLSI markets in the 1970s and 1980s.
  - Use fewer components & are much simpler to manufacture than TTL circuits.
- During this era, technology emerged that used P-MOS & N-MOS transistors in the same circuit.
  - Complementary MOS, or **CMOS**, technology.
- The CMOS INVERTER has two MOSFETs in series.
  - The P-channel device source is connected to V_{DD} .
  - The N-channel device has its source connected to ground—usually labeled V_{SS}.



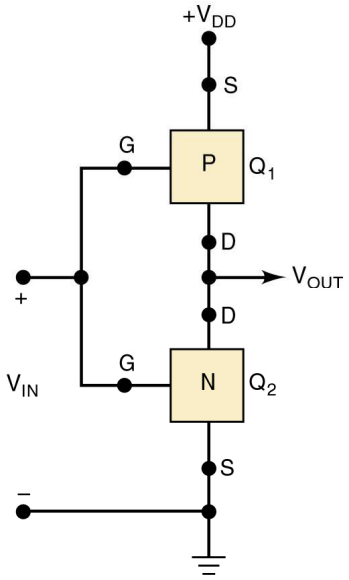
V_{IN}	Q_1	Q_2	V_{OUT}
$+V_{DD}$ (logic 1)	OFF $R_{OFF} = 10^{10}\ \Omega$	ON $R_{ON} = 1\ k\Omega$	$\simeq 0$ V
0 V (logic 0)	ON $R_{ON} = 1\ k\Omega$	OFF $R_{OFF} = 10^{10}\ \Omega$	$\simeq +V_{DD}$

$V_{OUT} = \overline{V_{IN}}$

Basic CMOS INVERTER.

CMOS Inverter

- The CMOS INVERTER has two MOSFETs in series.
  - Gates of the two devices are connected together as a common input.
  - Drains are connected together as common output.

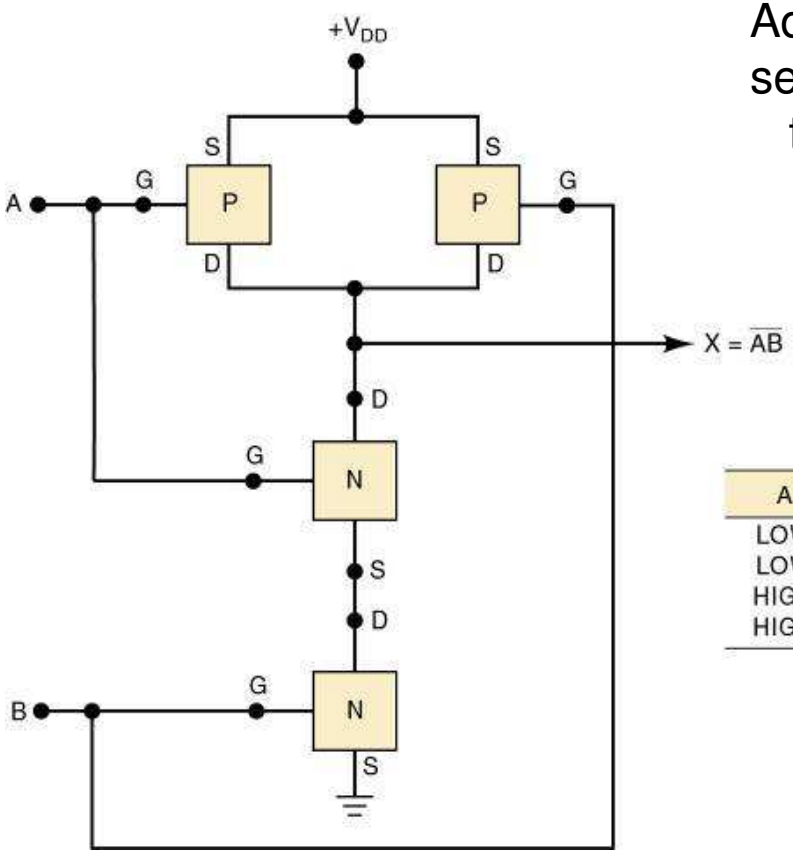


V_{IN}	Q_1	Q_2	V_{OUT}
$+V_{DD}$ (logic 1)	OFF $R_{OFF} = 10^{10}\ \Omega$	ON $R_{ON} = 1\ k\Omega$	$\simeq 0$ V
0 V (logic 0)	ON $R_{ON} = 1\ k\Omega$	OFF $R_{OFF} = 10^{10}\ \Omega$	$\simeq +V_{DD}$

$V_{OUT} = \overline{V_{IN}}$

Basic CMOS INVERTER.

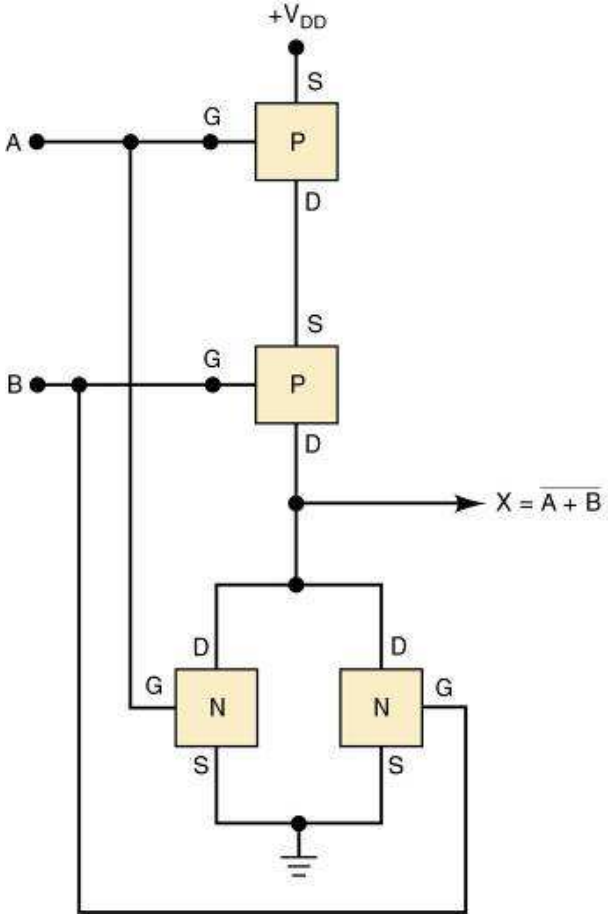
- A **NAND** gate is formed by modifying the basic INVERTER.



Adding parallel P-channel & series N-channel MOSFETs to the basic INVERTER.

A	B	X
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	LOW

- A CMOS **NOR** gate.



Formed by adding a series P-MOS and a parallel N-MOS to the basic INVERTER.

A	B	X
LOW	LOW	HIGH
LOW	HIGH	LOW
HIGH	LOW	LOW
HIGH	HIGH	LOW